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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/710,597

07/23/2004

Han-Chung Lai

13511-US-PA

4596

31561

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12/16/2005

EXAMINER

SOWARD, IDA M

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE

7 FLOOR-1, NO. 100

ROOSEVELT ROAD, SECTION 2

TAIPEI, 100

TAIWAN

ART UNIT

PAPER NUMBER

2822

DATE MAILED: 12/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary

Application No.

10/710,597

Applicant(s)

HAN-CHUNG LAI

Examiner

Ida M. Soward

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 November 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☒ Claim(s) 1,5,9 and 13 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 July 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the election filed November 25, 2005.

Election/Restrictions

Applicant's election without traverse of claims 1-16 in the reply filed on November 25, 2005 is acknowledged.

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

The abstract of the disclosure is objected to because “**comprising**” should have been **including** in line 1. Correction is required. See MPEP § 608.01(b).

Claim Objections

Claims 1, 5, 9 and 13 are objected to because of the following informalities:

1. in claims 1 and 9, “**transistor**” should have been **transistors** in line 6 of both claims; and
2. in claims 5 and 13, **layer** should have followed “**passivation**” in line 3 of both claims.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-7 and 9-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Watanabe et al. (US 2004/0250878 A1).

In regard to claim 1, Watanabe et al. teach A thin film transistor array, comprising: a substrate 311; a plurality of scan lines 3a (also in 321a) disposed over the substrate 311; a plurality of data lines 6a (also in 321a) disposed over the substrate 311, wherein the substrate 311 is defined into a plurality of pixel areas by the scan lines 3a and the data lines 6a; a plurality of thin film transistors 321a driven by the scan lines 3a and the data lines 6a, wherein each thin film transistor is disposed in one of the pixel areas correspondingly; an etching stop layer 65 disposed over the scan lines 3a ,wherein the etching stop layer (in 321a) has a plurality of openings; and a plurality of pixel electrodes 331, each pixel electrode 331 is disposed in one of the pixel areas and is electrically connected to one

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of the thin film transistors 321a correspondingly, wherein a portion of each pixel electrode 331 is coupled to one of the scan lines 3a through one of the openings to form a storage capacitor 30 (Figures 7-8 and 10, pages 5-6, paragraphs [0078]-[0084] and [0092]-[0097], respectively).

In regard to claim 2, Watanabe et al. teach a gate insulator disposed between the etching stop layer (in 321a) and the scan line (in 321a) (Figures 7-8 and 10, pages 5-6, paragraphs [0078]-[0084] and [0092]-[0097], respectively).

In regard to claim 3, Watanabe et al. teach the gate insulator (in 321a) having a plurality of recesses, and each recess is located under one of the openings of the etching stop layer (in 321a) (Figures 7-8 and 10, pages 5-6, paragraphs [0078]-[0084] and [0092]-[0097], respectively).

In regard to claim 4, Watanabe et al. teach a semiconductor layer (in 321a) disposed between the etching stop layer (in 321a) and the gate insulator (in 321a) (Figures 7-8 and 10, pages 5-6, paragraphs [0078]-[0084] and [0092]-[0097], respectively).

In regard to claim 5, Watanabe et al. teach a passivation layer (in 321a) disposed over the etching stop layer (in 321a) and the gate insulator (in 321a), wherein the openings of the etching stop layer (in 321a) is exposed by the passivation (Figures 7-8 and 10, pages 5-6, paragraphs [0078]-[0084] and [0092]-[0097], respectively).

In regard to claim 6, Watanabe et al. teach the etching stop layer (in 321a) comprising a plurality of stripe patterns, each stripe pattern is located above one of the

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scan lines (in 321a) correspondingly (Figures 7-8 and 10, pages 5-6, paragraphs [0078]-[0084] and [0092]-[0097], respectively).

In regard to claim 7, Watanabe et al. teach the etching stop layer (in 321a) comprising a plurality of frame patterns, each frame pattern is located under one of the pixel electrodes (in 321a) correspondingly (Figures 7-8 and 10, pages 5-6, paragraphs [0078]-[0084] and [0092]-[0097], respectively).

In regard to claim 9, Watanabe et al. teach a thin film transistor array, comprising: a substrate 311; a plurality of scan lines 3a (or in 321a) disposed over the substrate 311; a plurality of data lines 6a (or in 321a) disposed over the substrate 311, wherein the substrate is defined into a plurality of pixel areas by the scan lines 3a and the data lines 6a; a plurality of thin film transistor 321a driven by the scan lines 3a and the data lines 6a, wherein each thin film transistor is disposed in one of the pixel areas correspondingly; a plurality of common lines (in 321a) disposed over the substrate 311, wherein each common line (in 321a) is located between two adjacent scan lines 3a; an etching stop layer (in 321a) disposed over the common lines (in 321a) wherein the etching stop layer (in 321a) has a plurality of openings; and a plurality of pixel electrodes 331, each pixel electrode 331 is disposed in one of the pixel areas and is electrically connected to one of the thin film transistors 321a correspondingly, wherein a portion of each pixel electrode 331 is coupled to one of the scan lines (in 321a) through one of the openings to form a storage capacitor 30 (Figures 7-8 and 10, pages 5-6, paragraphs [0078]-[0084] and [0092]-[0097], respectively).

In regard to claim 10, Watanabe et al. teach a gate insulator (in 321a) disposed between the etching stop layer (in 321a) and the common line (in 321a) (Figures 7-8 and 10, pages 5-6, paragraphs [0078]-[0084] and [0092]-[0097], respectively).

In regard to claim 11, Watanabe et al. teach the gate insulator (in 321a) having a plurality of recesses (in 321a), and each recess is locating under one of the openings of the etching stop layer (in 321a) (Figures 7-8 and 10, pages 5-6, paragraphs [0078]-[0084] and [0092]-[0097], respectively).

In regard to claim 12, Watanabe et al. teach a semiconductor layer (in 321a) disposed between the etching stop layer (in 321a) and the gate insulator (in 321a) (Figures 7-8 and 10, pages 5-6, paragraphs [0078]-[0084] and [0092]-[0097], respectively).

In regard to claim 13, Watanabe et al. teach a passivation layer (in 321a) disposed over the etching stop layer (in 321a) and the gate insulator (in 321a), wherein the openings of the etching stop layer is exposed by the passivation (Figures 7-8 and 10, pages 5-6, paragraphs [0078]-[0084] and [0092]-[0097], respectively).

In regard to claim 14, Watanabe et al. teach the etching stop layer (in 321a) comprising a plurality of stripe patterns, each stripe pattern is located above one of the common lines (in 321a) correspondingly (Figures 7-8 and 10, pages 5-6, paragraphs [0078]-[0084] and [0092]-[0097], respectively).

In regard to claim 15, Watanabe et al. teach the etching stop layer (in 321a) comprising a plurality of frame patterns, each frame pattern is located under on of the

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pixel electrodes 331 correspondingly (Figures 7-8 and 10, pages 5-6, paragraphs [0078]-[0084] and [0092]-[0097], respectively).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 8 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al. (US 2004/0250878 A1) in view of Kim (US 6,262,784 B1).

Watanabe et al. teach all mentioned in the rejection above.

However, Watanabe et al. fail to teach a material of the pixel electrodes comprising ITO or IZO.

Kim teaches a material of the pixel electrodes comprising ITO (Figures 1-3, column 2, lines 35-46).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the thin film transistor array structure as taught by Watanabe et al. with the thin film transistor array having a material of the pixel electrodes comprising ITO as taught by Kim to provide improved liquid crystal display devices (column 3, lines 43-45).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to thin film transistor arrays:

Jeong et al. (US 2002/0151174 A1)	Kobashi (US 2002/0158573 A1)
Lim et al. (US 2002/0171108 A1)	Tsujimura et al. (US 2002/0190253 A1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M. Soward whose telephone number is 571-272-1845. The examiner can normally be reached on Monday - Thursday 6:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra V. Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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IMS

December 11, 2005

John M. Saward
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